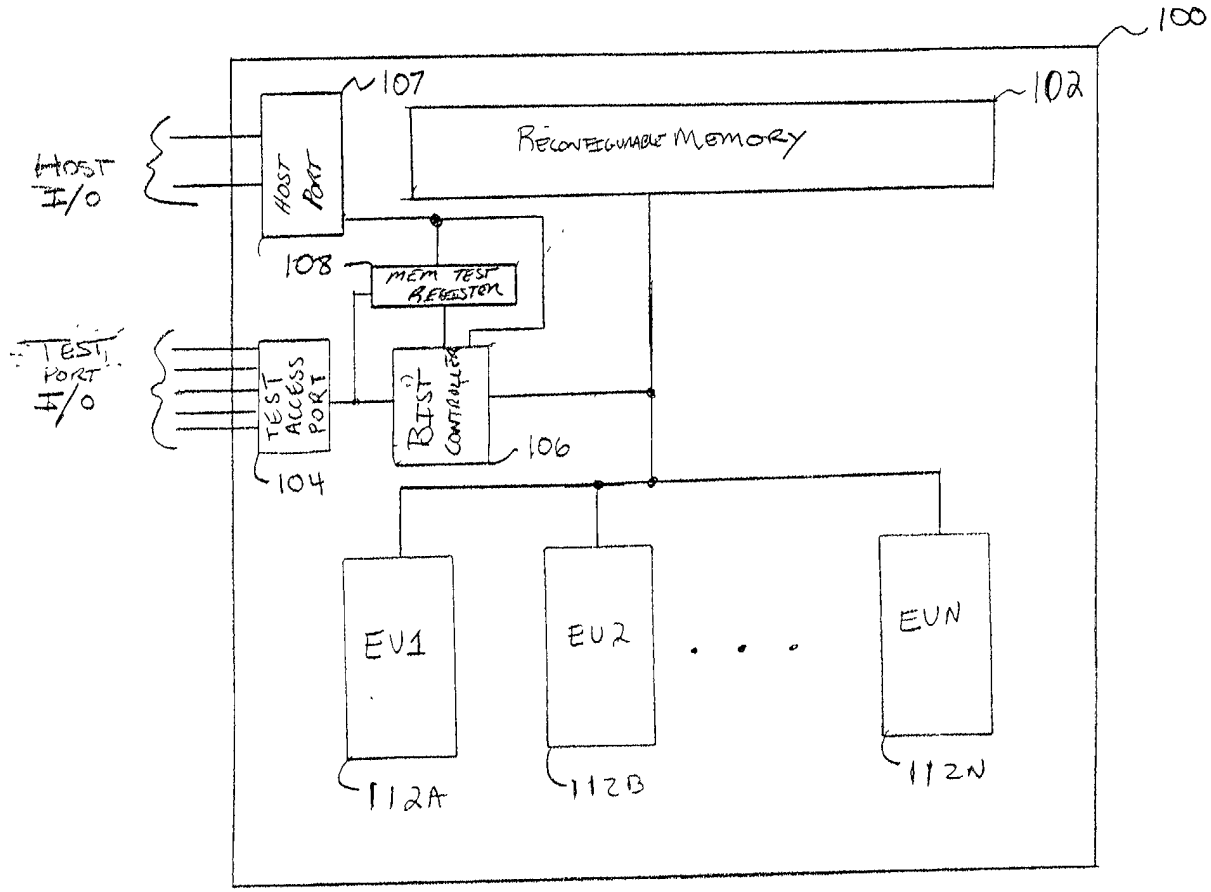

100
107
102
RECONFIGURABLE MEMORY
HOST I/O
HOST PORT
108
MEM TEST REGISTER
TEST PORT I/O
TEST ACCESS PORT
BIST CONTROLLER
106
104
EU1
EU2
EUN
112A
112B
112N

FIG. 1

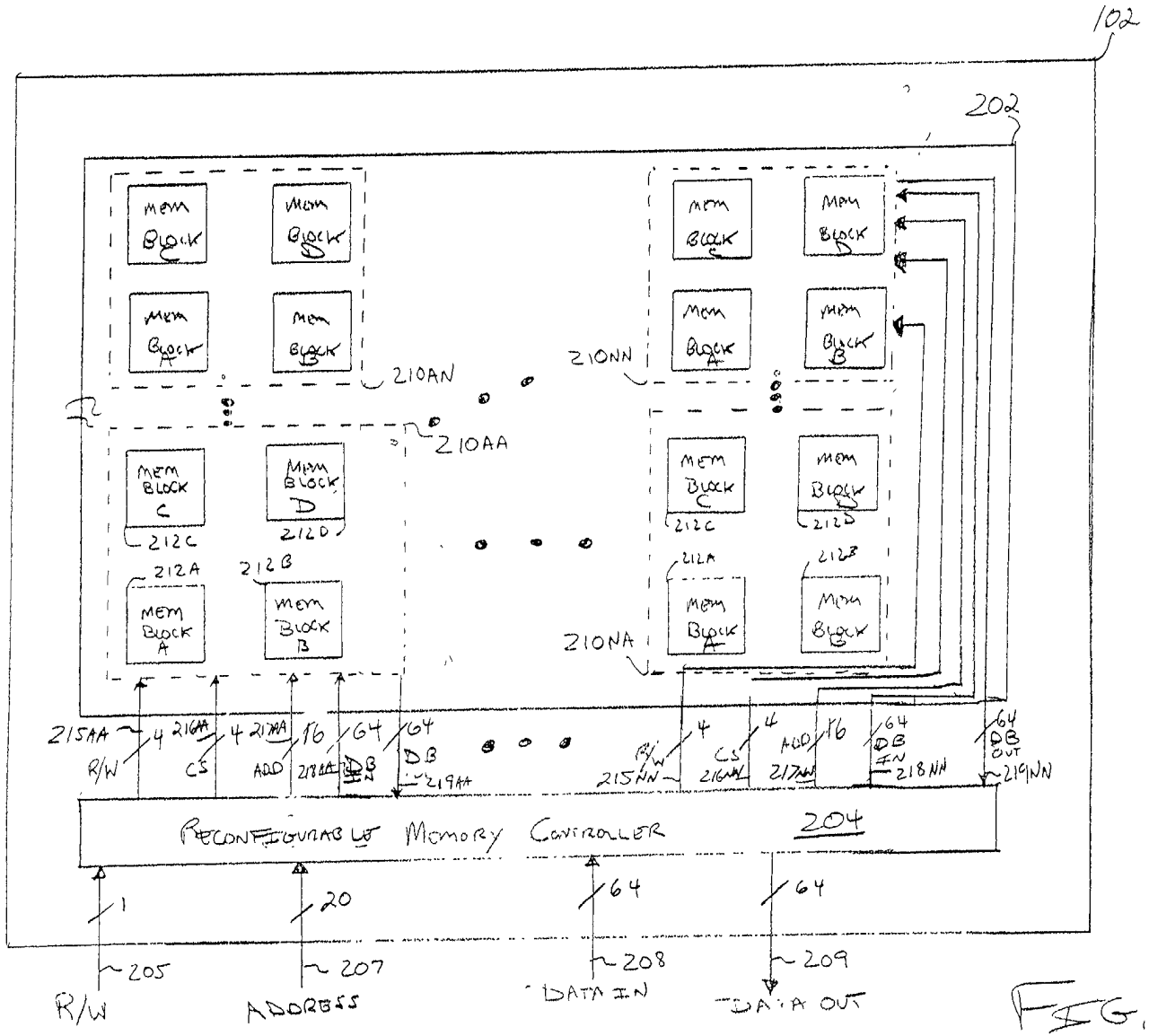

102
202
MEM BLOCK A
MEM BLOCK B
MEM BLOCK C
MEM BLOCK D
210AN
210AA
210NN
210NA
212A
212B
212C
212D
215AA
216AA
217AA
218AA
219AA
215NN
216NN
217NN
218NN
219NN
R/W
CS
ADD
DB IN
DB OUT
RECONFIGURABLE MEMORY CONTROLLER
204
205
207
208
209
R/W
ADDRESS
DATA IN
DATA OUT

FIG. 2

20120-2000

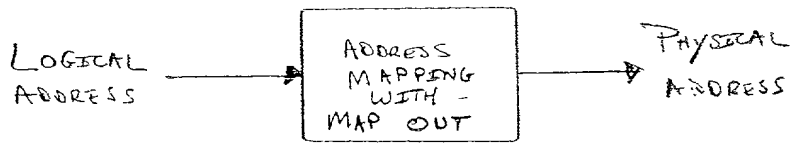



FIG. 3

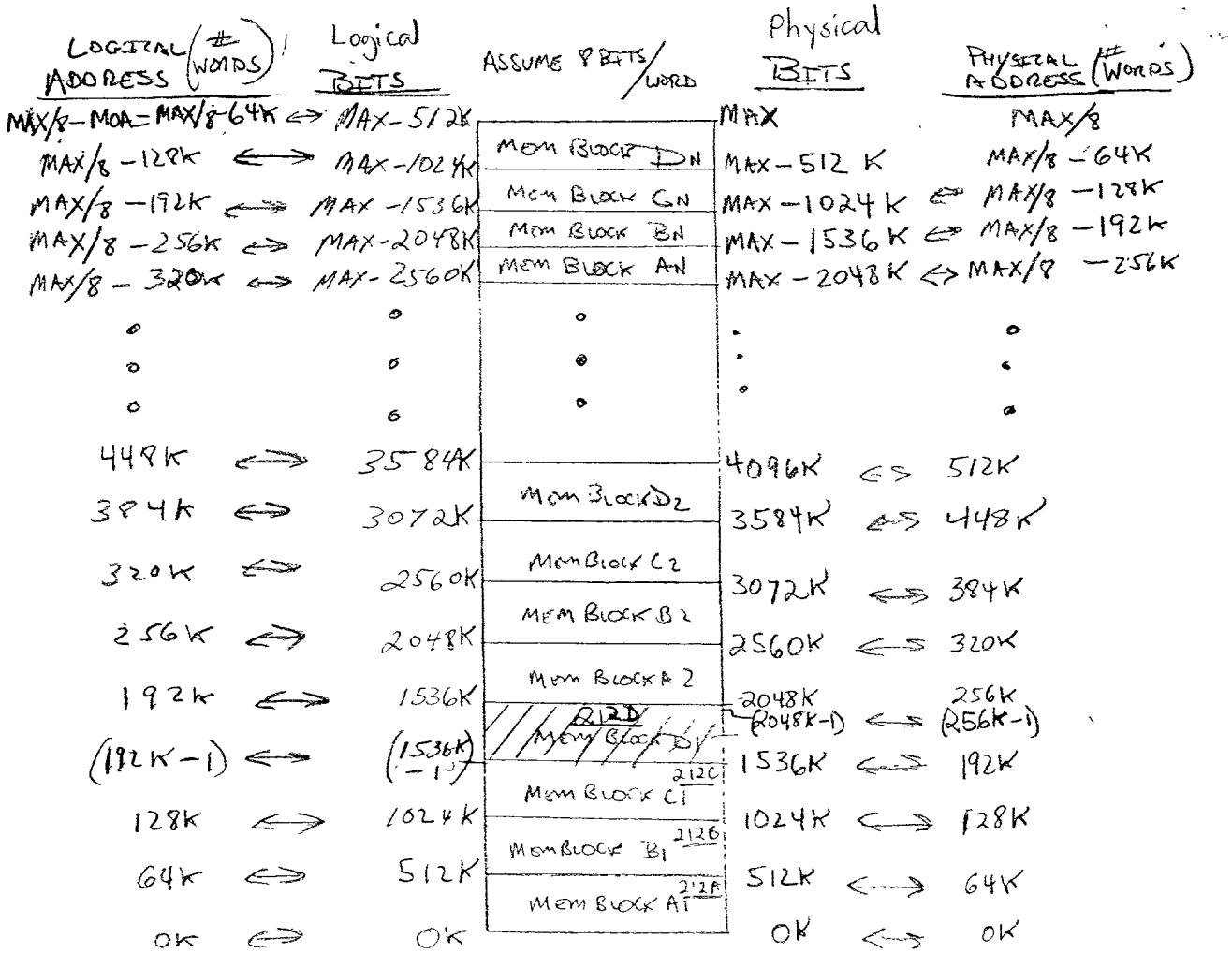



FIG. 4

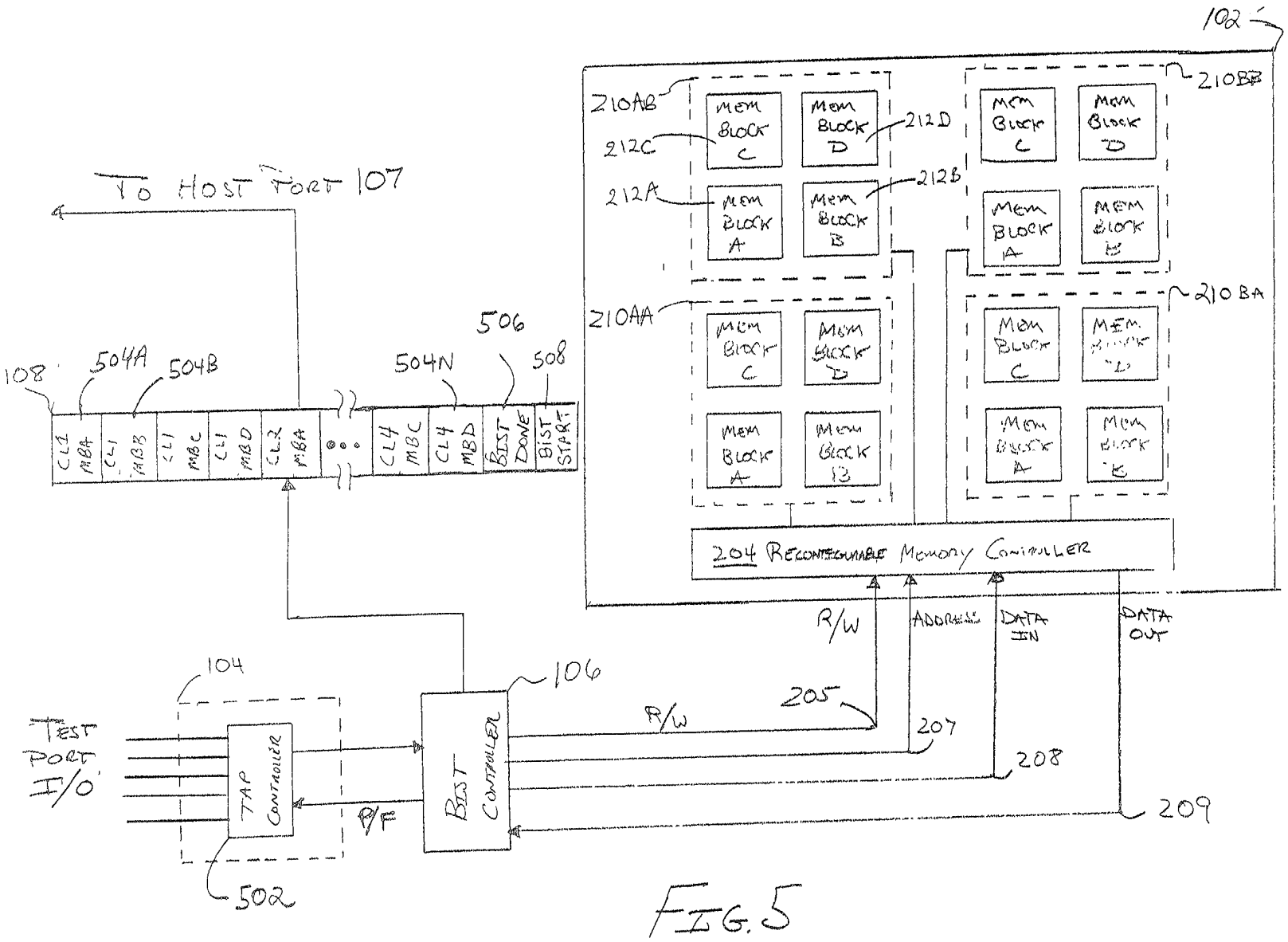
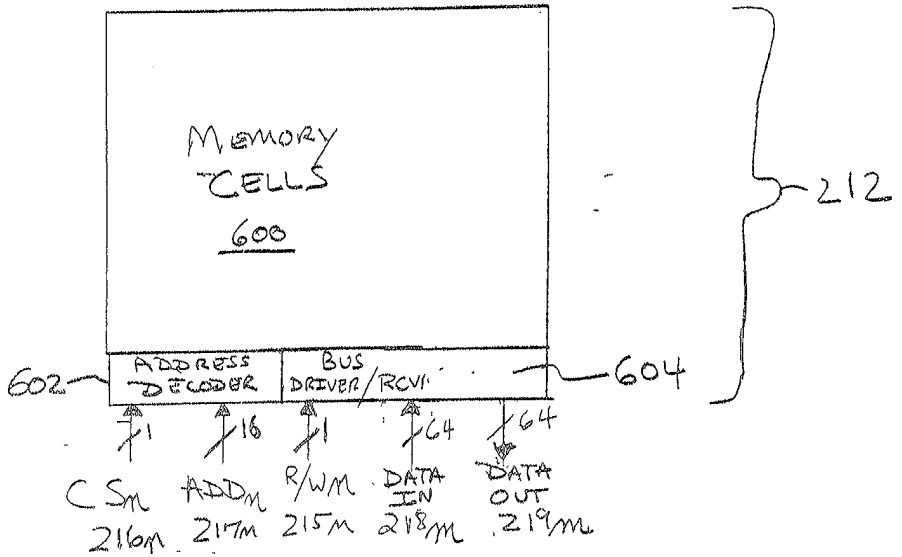

102
210AB
210BB
212C
212D
212A
212B
MEM BLOCK C
MEM BLOCK D
MEM BLOCK A
MEM BLOCK B
210AA
210BA
TO HOST PORT 107
108
504A
504B
504N
506
508
CL1 MBA
CL1 MBB
CL1 MBC
CL1 MBD
CL2 MBA
CL4 MBC
CL4 MBD
BIST DONE
BIST START
204 RECONFIGURABLE MEMORY CONTROLLER
R/W
ADDRESS
DATA IN
DATA OUT
104
106
TEST PORT I/O
TAP CONTROLLER
BIST CONTROLLER
205
207
208
209
502

FIG. 5

FIG. 6


MEMORY CELLS
600
212
602
ADDRESS DECODER
BUS DRIVER/RCVR
604
1
16
1
64
64
CSm
ADDm
R/Wm
DATA IN
DATA OUT
216m
217m
215m
218m
219m

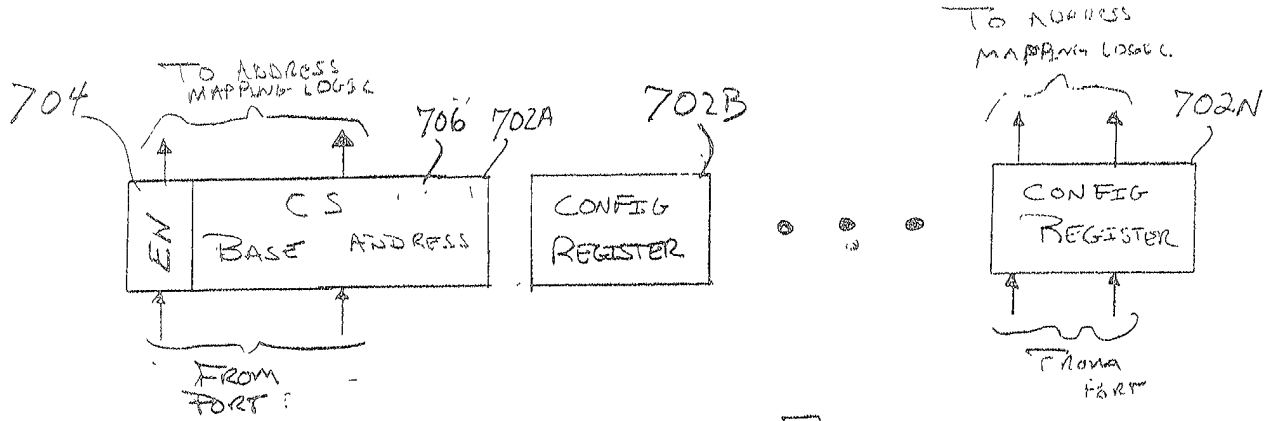

704
TO ADDRESS MAPPING LOGIC
706
702A
702B
TO ADDRESS MAPPING LOGIC
702N
EN
CS
BASE ADDRESS
CONFIG REGISTER
CONFIG REGISTER
FROM PORT
FROM PORT

FIG. 7

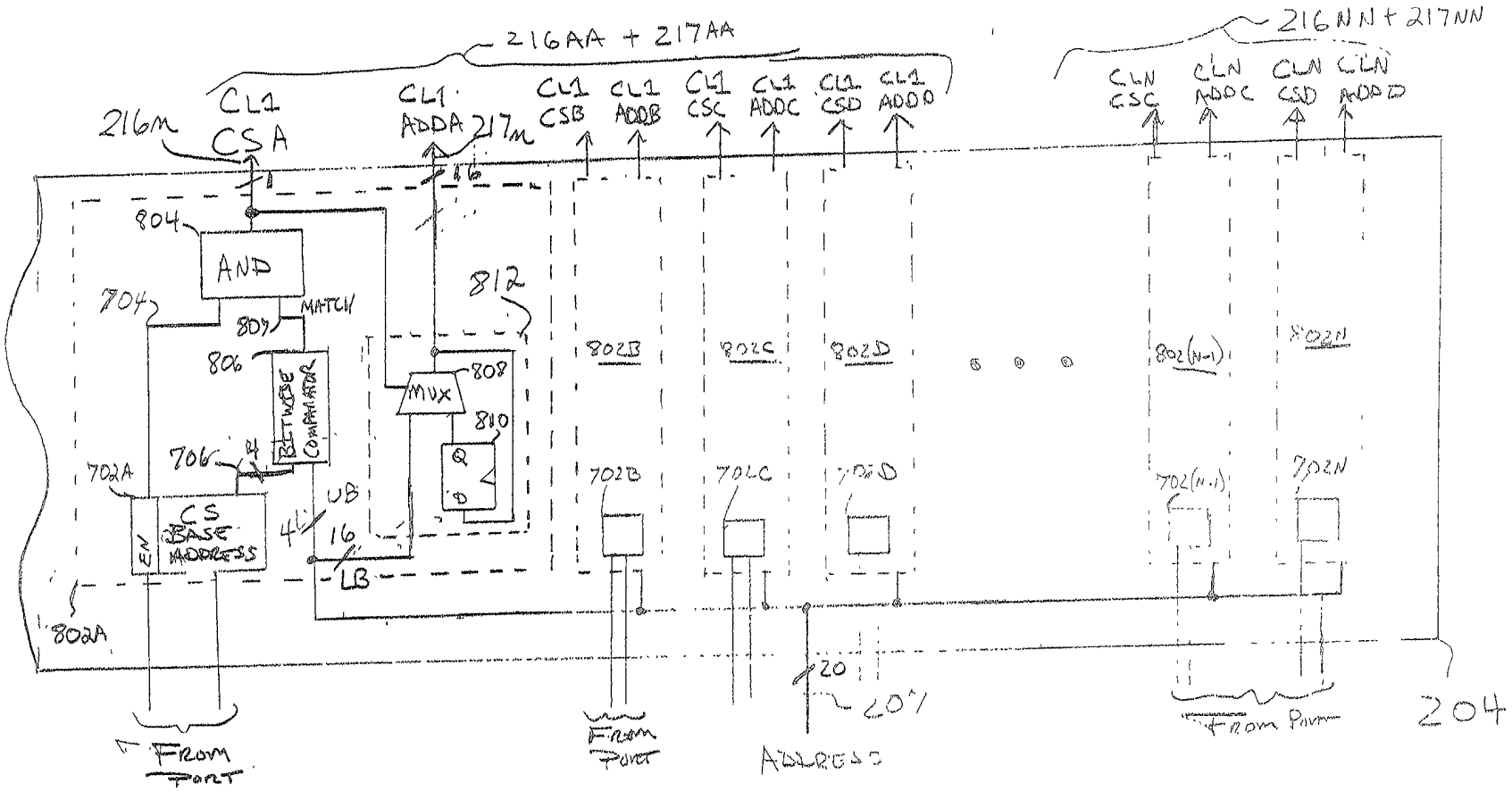

216AA + 217AA
216NN + 217NN
216M
CL1 CSA
CL1 ADDA
217M
CL1 CSB
CL1 ADDB
CL1 CSC
CL1 ADDC
CL1 CSD
CL1 ADDD
CLN CSC
CLN ADDC
CLN CSD
CLN ADDD
804
AND
704
MATCH
806
BITWISE COMPARATOR
812
MUX
808
810
Q
D
706
4
702A
CS
BASE ADDRESS
EN
UB
16
LB
802A
802B
802C
802D
802(N-1)
802N
702B
702C
702D
702(N-1)
702N
20
20'
From Port
From Port
Address
From Pmm
204

FIG. 8

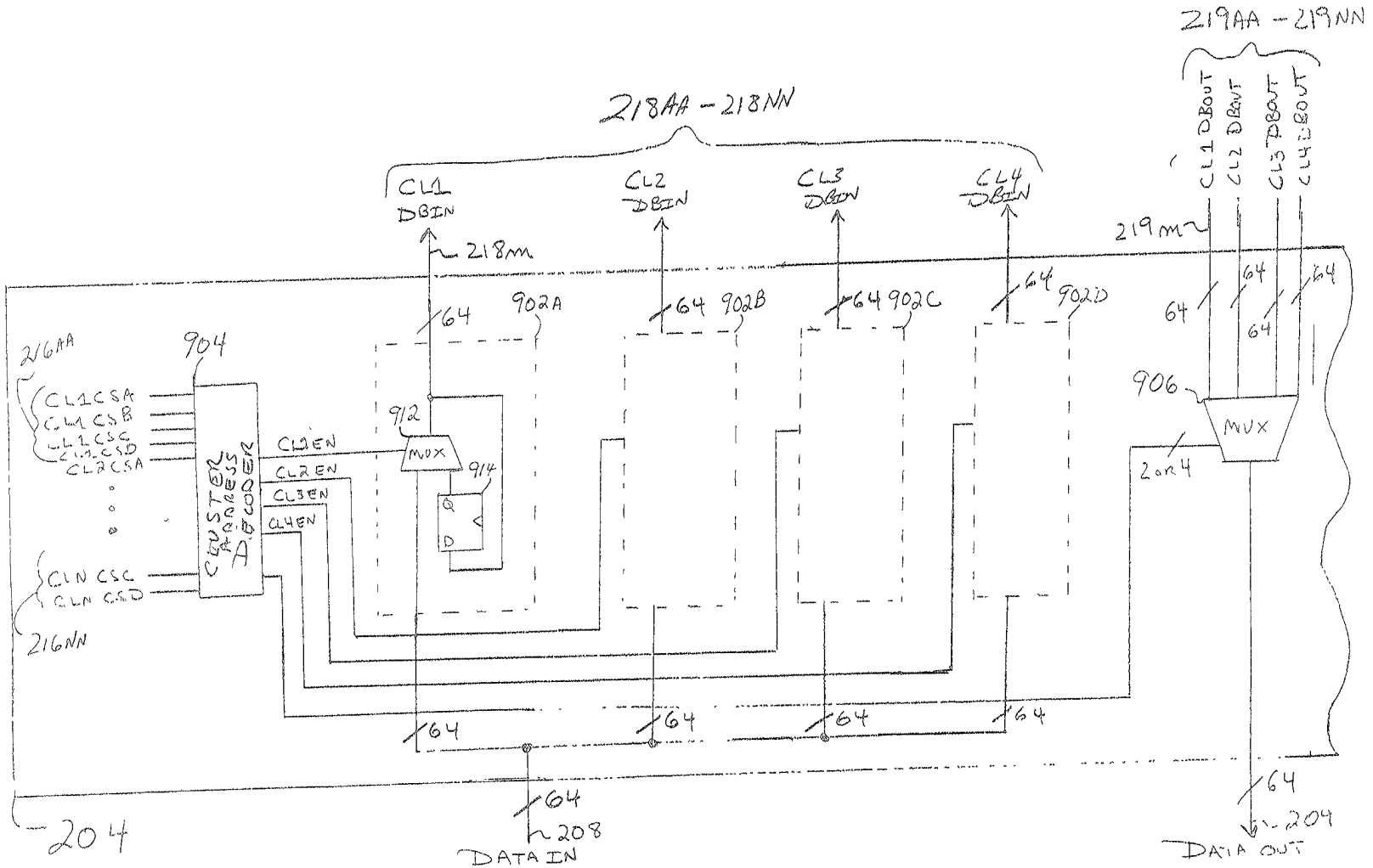

219AA - 219NN
218AA - 218NN
CL1 DBIN
CL2 DBIN
CL3 DBIN
CL4 DBIN
CL1 DBOUT
CL2 DBOUT
CL3 DBOUT
CL4 DBOUT
218m
219m
64
902A
902B
902C
902D
216AA
904
CL1CSA
CL1CSB
CL1CSC
CL1CSD
CL2CSA
CLN CSC
CLN CSD
216NN
CLUSTER ADDRESS DECODER
CL1EN
CL2EN
CL3EN
CL4EN
912
MUX
914
Q
D
906
2or4
204
208
DATA IN
DATA OUT

FIG. 9